Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Previously Presented) A method of programming a semiconductor memory device, comprising:

applying a set pulse continuously to the memory device, applying the set pulse to the memory device comprises applying a current to a bit line of the memory device;

while the set pulse is applied, detecting a state of the memory device; and

when the memory device is determined to be in a desired set state, removing the set pulse by removing the current applied to the bit line of the memory device, such that duration of the set pulse is controlled based on the state of the memory device.

2. (Original) The method of claim 1, wherein, when the memory device is in a reset state, a programmable material of the memory device is in an amorphous state.

3. (Original) The method of claim 1, wherein, when the memory device is in the set state, a programmable material of the memory device is in a crystalline state.

4. (Original) The method of claim 3, wherein, when the memory device is in a reset state, a programmable material of the memory device is in an amorphous state.

5. (Original) The method of claim 1, wherein detecting a state of the memory device comprises detecting a resistance in the device.

6. (Original) The method of claim 5, wherein the detected resistance comprises resistance in a programmable material of the memory device.

7. (Original) The method of claim 6, wherein resistance of the programmable material in an amorphous state of the programmable material is higher than resistance of the programmable material in a crystalline state of the programmable material.

8. (Previously Presented) The method of claim 1, wherein detecting a state of the memory device comprises detecting a voltage of the bit line of the memory device.

9. (Original) The method of claim 8, wherein applying a set pulse to the memory device comprises generating a control signal which controls application of the set pulse to the memory device.

10. (Original) The method of claim 9, wherein the control signal is generated to cause the set pulse to be activated in response to a write enable signal.

11. (Original) The method of claim 9, wherein the control signal is generated to cause the set pulse to be activated.

12. (Original) The method of claim 9, wherein the control signal is generated to cause the set pulse to be removed when the detected bit line voltage is below a reference voltage.

13. (Original) The method of claim 12, wherein the reference voltage is a set programming voltage of a programmable material in the memory device.

14. (Original) The method of claim 9, wherein the control signal is generated to cause the set pulse to be removed when the detected bit line voltage is equal to a reference voltage.

15. (Original) The method of claim 9, wherein, when the memory device is being programmed to a set state from a reset state, the control signal is generated to cause the set pulse to be applied while the memory device transitions from the reset state to the set state and removed after the transition.

16. (Original) The method of claim 9, wherein, when the memory device is being programmed to a set state from a reset state, the control signal is generated to cause the set pulse to be applied while the detected bit line voltage is above a reference voltage and removed after the detected bit line voltage drops below the reference voltage.

17. (Original) The method of claim 9, wherein, when the memory device is being programmed to a set state from the set state, the control signal is generated to be applied in response to a write enable signal and removed when it is determined that the detected bit line voltage is below a reference voltage.

18. (Original) The method of claim 9, wherein, when the memory device is being programmed to a set state from the set state, the control signal is generated to be applied in response to a write enable signal and removed when it is determined that the detected bit line voltage is equal to a reference voltage.

19. (Cancelled)

20. (Previously Presented) The method of claim 1, wherein detecting a state of the memory device comprises detecting a voltage of the bit line while the current is applied to the bit line.

21. (Original) The method of claim 1, wherein applying a set pulse to the memory device comprises generating a control signal which controls application of the set pulse to the memory device.

22. (Original) The method of claim 1, wherein the memory device comprises a phase change material.

23. (Original) The method of claim 22, wherein the phase change material comprises germanium, antimony and tellurium.

24. (Original) The method of claim 1, wherein the memory device comprises at least one chalcogenide element.

25. (Original) The method of claim 1, wherein a reset current in the memory device is greater than a set current in the memory device.

26. (Original) The method of claim 1, wherein a reset pulse width is narrower than a set pulse width.

27. (Currently Amended) A semiconductor memory device, comprising:

a detecting circuit for detecting a state of the memory device; and

a controller for continuously applying a set pulse to the memory device by continuously applying a [[set]] current to a bit line of the memory device, the controller removing the set pulse when the memory device is detected to be in a desired set state, such that duration of the set pulse is controlled based on the state of the memory device.

28. (Original) The semiconductor memory device of claim 27, further comprising a programmable material, wherein, in a first state, the programmable material is in an amorphous state.

29. (Original) The semiconductor memory device of claim 27, further comprising a programmable material, wherein, in a first state, the programmable material is in a crystalline state.

30. (Original) The semiconductor memory device of claim 29, wherein, in a second state, the programmable material is in an amorphous state.

31. (Currently Amended) The semiconductor memory device of claim 27, wherein the ~~detector~~detecting circuit detects a resistance in the device.

32. (Original) The semiconductor memory device of claim 31, wherein the detected resistance comprises resistance in a programmable material of the memory device.

33. (Previously Presented) The semiconductor memory device of claim 27, wherein the detecting circuit detects a voltage of the bit line of the memory device.

34. (Original) The semiconductor memory device of claim 33, wherein the detecting circuit comprises a sense amplifier.

35. (Original) The semiconductor memory device of claim 34, wherein the sense amplifier compares the voltage of the bit line to a reference voltage.

36. (Original) The semiconductor memory device of claim 35, wherein the reference voltage is a set programming voltage of a programmable material in the memory device.

37. (Original) The semiconductor memory device of claim 33, wherein the controller further comprises a control signal generator for generating a control signal which controls application of the set pulse to the memory device.

38. (Original) The semiconductor memory device of claim 37, wherein the control signal is generated to cause the set pulse to be activated in response to a write enable signal.

39. (Original) The semiconductor memory device of claim 37, wherein the control signal is generated to cause the set pulse to be activated.

40. (Original) The semiconductor memory device of claim 37, wherein the control signal is generated to cause the set pulse to be removed when the detected bit line voltage is below a reference voltage.

41. (Original) The semiconductor memory device of claim 37, wherein the control signal is

generated to cause the set pulse to be removed when the detected bit line voltage is equal to a reference voltage.

42. (Original) The semiconductor memory device of claim 37, wherein, when the memory device is being programmed to a set state from a reset state, the control signal is generated to cause the set pulse to be applied while the memory device transitions from the reset state to the set state and removed after the transition.

43. (Original) The semiconductor memory device of claim 37, wherein, when the memory device is being programmed to a set state from a reset state, the control signal is generated to cause the set pulse to be applied while the detected bit line voltage is above a reference voltage and removed after the detected bit line voltage drops below the reference voltage.

44. (Original) The semiconductor memory device of claim 37, wherein, when the memory device is being programmed to a set state from the set state, the control signal is generated to be applied in response to a write enable signal and removed when it is determined that the detected bit line voltage is below a reference voltage.

45. (Original) The semiconductor memory device of claim 37, wherein, when the memory device is being programmed to a set state from the set state, the control signal is generated to be applied in response to a write enable signal and removed when it is determined that the detected bit line voltage is equal to a reference voltage.

46. (Previously Presented) The semiconductor memory device of claim 27, further comprising a driver for applying the current to the bit line of the memory device.

47. (Currently Amended) The semiconductor memory device of claim [[1]]46, wherein the driver applies a set current to the bit line in response to a set enable signal.

48. (Currently Amended) The semiconductor memory device of claim [[1]]46, wherein the

driver applies a reset current to the bit line in response to a reset enable signal.

49. (Currently Amended) The semiconductor memory device of claim [[46]]27, wherein the ~~detector~~detecting circuit detects a voltage of the bit line while the current is applied to the bit line.

50. (Original) The semiconductor memory device of claim 27, wherein the controller further comprises a control signal generator which generates a control signal which controls application of the set pulse to the memory device.

51. (Original) The semiconductor memory device of claim 27, wherein the memory device comprises a phase change material.

52. (Original) The semiconductor memory device of claim 51, wherein the phase change material comprises germanium, antimony and tellurium.

53. (Original) The semiconductor memory device of claim 27, wherein the memory device comprises at least one chalcogenide element.

54. (Original) The semiconductor memory device of claim 27, wherein a reset current in the memory device is greater than a set current in the memory device.

55. (Original) The semiconductor memory device of claim 27, wherein a reset pulse width is narrower than a set pulse width.